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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/551,790	04/18/2000	William Garvin Holland	RALS9-2000-0057US1	2608

25299 7590 03/10/2005

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EXAMINER	
LANE, JOHN A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/551,790	HOLLAND ET AL.	
	Examiner	Art Unit	
	Jack A Lane	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) *5-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the RCE and amendment filed 12/17/2004. Claims 1-4 are presented for examination. Claims 5-6 are withdrawn from further consideration. Any objections or rejections made in the previous office action not specifically repeated below are withdrawn or have been overcome by applicant's response.

2. This application contains claim 5-6 drawn to an invention nonelected with traverse in Office action mailed 12/03/2003. A complete reply to a final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103 (a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any

inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103(a).

4. Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Minyard et al. (Pat. No. 6,487,606) in view of Bass et al. (Pat. No. 6,460,120).

Minyard teaches a network system as shown in figure 2. The claimed "central processing unit" corresponds to one of CPU's 22, 24, 26 and 28 shown in figure 2. The claimed "plurality of peripheral devices...comprising volatile memory, non-volatile memory, and a plurality of I/O subsystems" corresponds to the input and output devices, volatile and non-volatile memory discussed at column 2, lines 45-46. The claimed "peripheral devices" can also correspond to any devices coupled to one of co-processors 62,64,66 and 68 through network 30. The claimed "network processor" corresponds to one of co-processors 62, 64, 66 and 68. The claimed "data memory" corresponds to one or more buffers 52, 54, 56 and 58. The co-processors function as a front end interface between the network 30 and the CPUs as discussed at column 4, lines 1-2. The co-processors also relieve the CPU's of processing overhead thereby freeing the CPU's to perform other tasks more efficiently and quickly (col. 4, line 66 – col. 5,

line 13). However, a single co-processor/network processor is not taught as having a plurality of interface processors.

Bass is introduced for its teaching of a network processor 10 (fig 1 and 12b). It is noted that the network processors of figures 3 and 4 correspond identically to the network processor of figures 1 and 18, respectively of Bass. The claimed "peripheral devices" can also correspond D-RAMs (2-7), S-RAM(1) and Data Store (4). The claimed "plurality of interface processors" correspond to processors including the ten protocol processors shown in figure 12b. The claimed "data memory" corresponds to DRAM and SRAM shown in figure 1. Data flow handling and flexibility is enhanced using the network processor of Bass.

Because the network processor of Bass provides improved data flow handling and flexibility as a result of the plural processor design, it would have been obvious to use such a network processor in the network system of Minyard to perform the network operations (i.e. data handling, overhead tasks etc.) otherwise performed by the CPU's. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

The dependent claim features, while part of the invention, appear to be well known and their relevance not essential to the main invention found in the

independent claim(s). Thus, a detailed discussion of the well known claim feature(s) is not warranted at this time. Applicant is invited to comment on any claim feature(s) deemed to be patentably distinguishable from the prior art.

In the Remarks filed 06/03/03, at page 4, applicant argues:

> Taking note that, importantly, the entire claim 1 is directed to "a computer system" and nowhere mentions a network or any communication external to the computer system.

In response, the claimed "central processing unit" and "network processor" are stated as corresponding to one or more CPU's 22, 24, 26 and 28 and one or more co-processors 62, 64, 66 and 68, respectively (see rejection, section 6). Thus, the claimed "computer system" can correspond to any one of host processors 12, 14, 16 and 18, including CPU's and co-processors irrespective of network 30.

Applicant argues further the following claim features are not found in the prior art:

> a network processor operatively interposed between said central processing unit and said peripheral devices and among said peripheral devices
>
> said network processor cooperating with said central processing unit in directing the exchange of data between said input/output ports and the flow of data through said data memory to and from said volatile memory and said non-volatile memory...

In response, Bass teaches a network processor/interface device (IDC) (10) (see figures 2) connected between a system processor and peripheral devices

(DRAM, SRAM, EEPROM, flash memory). Data is transferred between the input/output ports coupled to the system processor and through data store 4 (figure 1) to DRAM/SRAM/EEPROM/flash memory.

Applicant argues:

> Claim 2...is further patentable...by requiring that the network processor be formed on a single semiconductor substrate

In response, Bass teaches a single substrate 10 (col. 6, lines 34-36)

In the Remarks filed 12/17/2004, applicant argues:

> The co-processors of Minyard are not "operatively interposed between said central processing unit and said peripheral devices and among said peripheral devices"

In response, figure 1 clearly shows a co-processor (62,64,66 or 66) operatively interposed between a central processing unit (22, 24, 26 or 28) and peripheral devices (i.e. memory) coupled to other host processors 12, 14, 16 or 18. The peripheral devices can also correspond to D-RAMs (2-7), S-RAM (1) and/or Data Store (4).

5. Applicant's arguments filed 12/17/2004 have been fully considered but they are not deemed to be persuasive.

Please find the amended rejection above in section 4.

Any response to this action should be mailed to:

Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for Official communications intended for entry)

Or:

(703) 872-9306, (for Non-Official or draft communications, please label "Non-Official" or "DRAFT")

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack A. Lane whose telephone number is 571 272-4208. The examiner can normally be reached on Mon-Fri from 7:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571 272-4210.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571 272-2100

JACK A. LANE
PRIMARY EXAMINER